II. AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior listings, or versions, of claims.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously presented) A system for determining timing in an electrical circuit comprising:
    a. a netlist input for receiving a circuit netlist representing a topology of the electrical circuit to be timed;
    b. an assertion input for receiving a set of one or more assertions representing boundary timing conditions;
    c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of variation;
    d. a model input for receiving parameterized delay models, each parameterized delay model containing one or more models for a delay of one or more components of the electrical circuit, each model being a function of one or more of the sources of delay variation; and
    e. a process that determines and outputs a statistical arrival time of one or more nodes of the electrical circuit, the statistical arrival time being in a

form of a weighted sum of probability distributions of one or more of the sources of variation.

2. (Original) A system, as in claim 1, where the process determines the statistical arrival times by visiting each node of the electrical circuit only once.

3. (Previously presented) A system, as in claim 1, where the system further determines and outputs a statistical required arrival time of one or more nodes of the electrical circuit, the statistical required arrival time being in a form of a weighted sum of probability distributions of one or more of the sources of variation.

4. (Previously presented) A system, as in claim 1, where the process further determines and outputs a statistical slack of one or more nodes of the electrical circuits, the statistical slack being in a form of a weighted sum of probability distributions of one or more of the sources of variation.

5. (Original) A system, as in claim 1, where the process determines and outputs a statistical slew of one or more nodes of the electrical circuits, the statistical slew being in the form of a weighted sum of probability distributions of one or more of the sources of variation.

6. (Previously presented) A system, as in claim 1, where the process further performs a late mode statistical timing analysis and outputs late mode arrival times.

7. (Previously presented) A system, as in claim 1, where the process further performs an early mode statistical timing analysis and outputs one or more early mode arrival times.

8. (Previously presented) A system, as in claim 1, where one or more separate rising and falling statistical delays are provided for each component of the electrical circuit and the process further determines and outputs one or more separate rising and falling statistical arrival times for one or more nodes of the electrical circuit.

9. (Previously presented) A system, as in claim 8, where the process further determines and outputs one or more of the separate rising and falling statistical required arrival times, one or more separate rising and falling statistical slacks, and one or more separate rising and falling statistical slews for one or more nodes of the electrical circuit.

10. (Original) A system, as in claim 1, where the electrical circuit is one or more of the following: a combinational circuit, a sequential circuit, a static logic circuit, and a dynamic logic circuit.

11. (Original) A system, as in claim 1, where the electrical circuit is a sequential circuit that contains one or more of the following: an edge-triggered latch, a master-slave latch, a level-sensitive latch, and a transparent latch.

12. (Original) A system, as in claim 1, where the circuit contains multiple clock phases.

13. (Original) A system, as in claim 1, where the parameterized delay model for each component of the electrical circuit comprises one or more of: a deterministic part, a correlated part, and an independently random part.

14. (Original) A system, as in claim 13, where the sources of variation are correlated.

15. (Original) A system, as in claim 13, where the sources of variation are independent.

16. (Original) A system, as in claim 1, where the parameterized delay models are pre-stored in a table in one or more memories of the system.

17. (Original) A system, as in claim 1, where the parameterized delay models are pre-stored as coefficients of delay equations in one or more memories of the system.

18. (Original) A system, as in claim 1, where the parameterized delay models are determined by circuit simulation on-the-fly.

19. (Original) A system, as in claim 1, where each assertion is one of deterministic and statistical.

20. (Canceled)

21. (Canceled)

22-43. (Canceled)

44. (Original) A system for analyzing timing of an electrical circuit, comprising:

a. means for reading the netlist, assertions, parameterized delay models and list of sources of variation;

b. means for building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. means for levelizing the graph for forward propagation of statistical arrival times; and

d. at each level of the timing graph, means for propagating one or more statistical arrival times at each of the nodes, each of the statistical arrival times being a weighted sum of probability distributions of one or more of the sources of variation.

45. (Previously presented) A system, as in claim 44, further comprising:

e. means for levelizing the graph for backward propagation of statistical required arrival times; and

f. at each level of the timing graph, means for propagating one or more statistical required arrival times at each of the nodes, each of the statistical required arrival times being a weighted sum of probability distributions of one or more of the sources of variation.

46-47. (Canceled)